High Performance Extraction of 2.5D/3D-IC Package

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Outline

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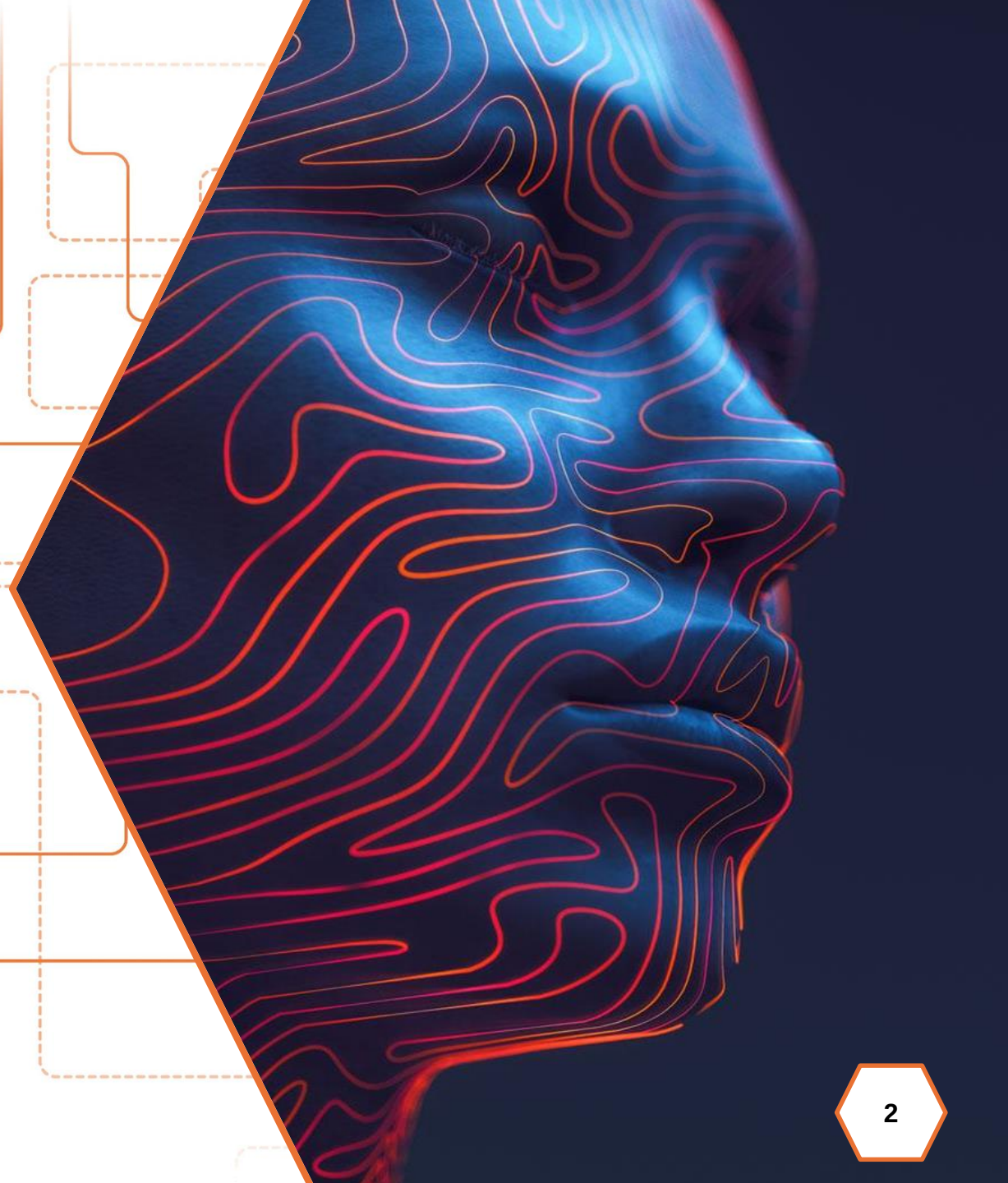
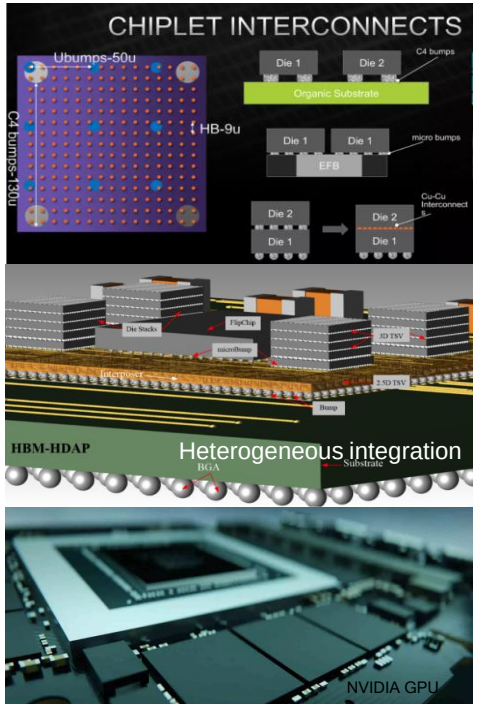
- High Performance Hybrid Electromagnetic Solver
- Machine Learning Models
- Performance and Validation
- System Level Co-design Automation Flow
- Summary



Challenges

- Complexity with 2.5D/3D-IC design
  - Extreme pin count
    - Huge pin count >10K
  - Smaller metal dimension
    - Bump pitch <30um
    - Layer Thickness <2um
    - Metal trace/spacing <2um
  - Different design structure
    - Cluster via/TIV/TSV
    - Bias table
    - Degassing hole
  - Chip-level electrical parameter
    - IC related parasitic parameters
    - Electrical Migration
  - 10x components & larger PKG size
    - Tens of dies & LSI/IPD are in a package
    - Larger overall package size > 2500 mm^2
  - Adaptive PKG stackup
    - 2.5D package, side by side package
    - 3D stacking, package on package
    - Embedded design, LSI, IPD

Extension of Moore's law

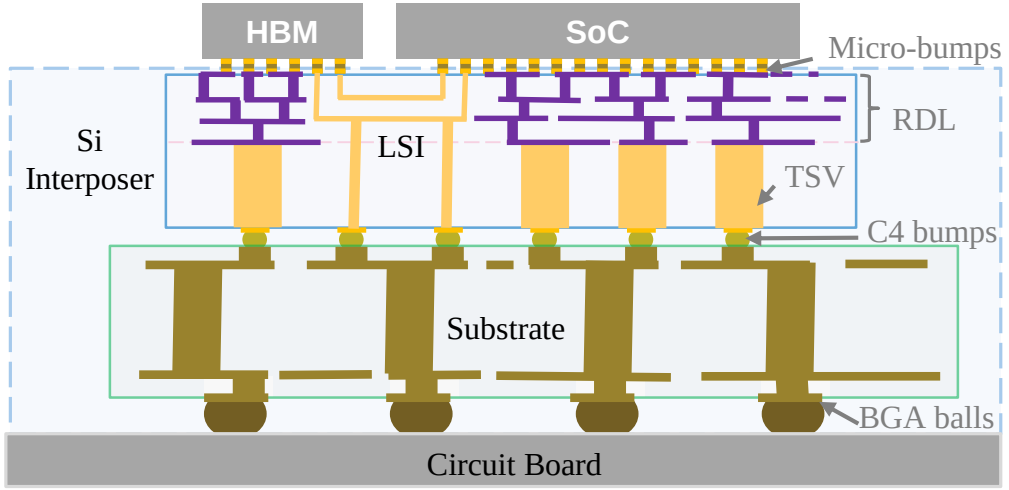


Intelligent Advanced IC Package Extractor

- Hybrid electromagnetic (EM) solver

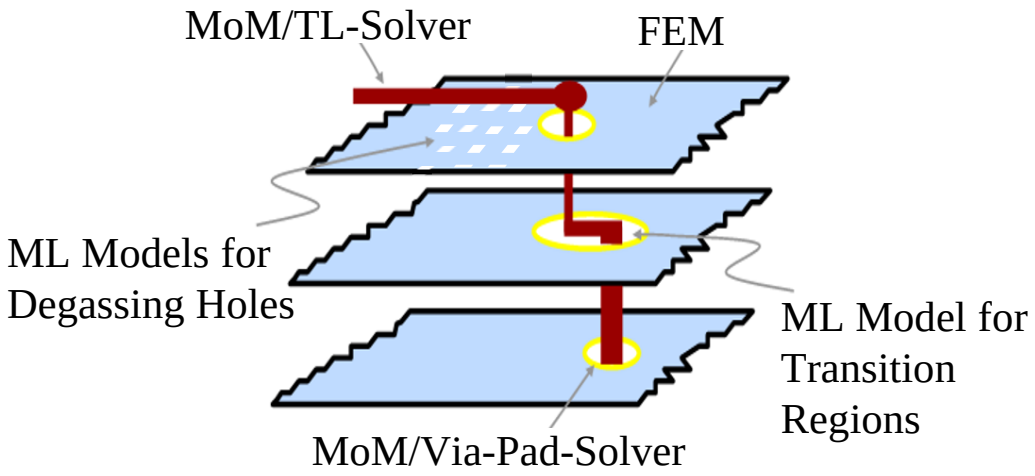
  Advanced IC package is a complex layered system composed of various chiplets interconnected by hybrid bonding, interpose with TSVs and RDLs with traces and shapes for vertical and lateral communications, substrate with build-up interconnects, etc.

  - Different basic EM solvers for modeling different parts to fully utilized advantages of various EM methods
  - Leveraging machine learning (ML) techniques to simplify the extraction complexity and improve accuracy

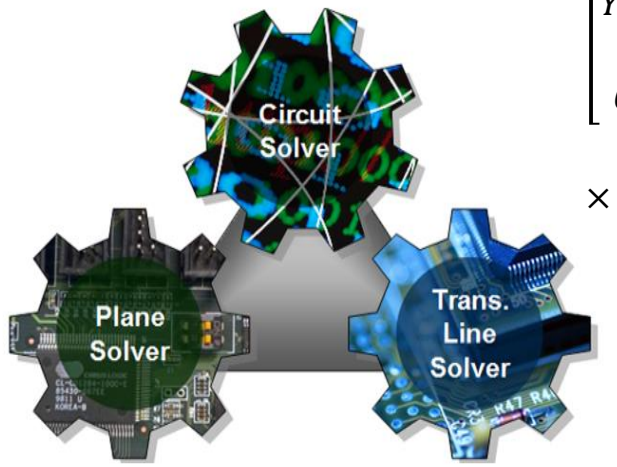


Intelligent Advanced IC Package Extractor

- Hybrid electromagnetic (EM) solver
  - Fields are separated to parallel-planes fields and transmission line fields of traces, vias, pads, etc.
  - Field-circuit coextraction



Circuit & discontinuity models



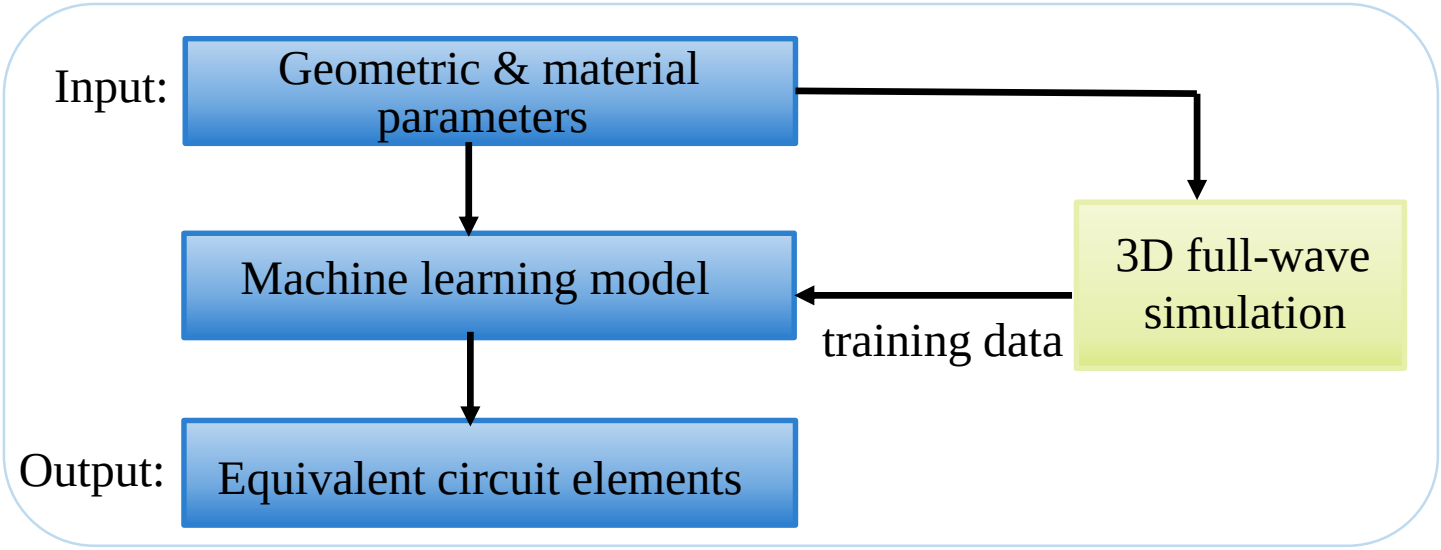
$$\begin{bmatrix} Y_{FEM} & 0 & C_{fc} \\ 0 & Y_{circuit} & I \\ C_{cf} & I & 0 \end{bmatrix} \times \begin{bmatrix} E \\ V_{circuit} \\ I_{circuit} \end{bmatrix} = \begin{bmatrix} 0 \\ I_S \\ 0 \end{bmatrix}$$

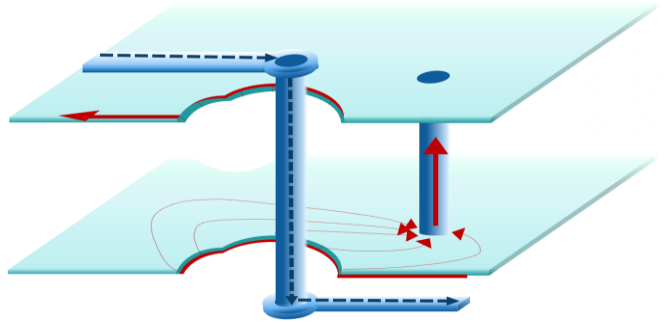
Plane & medium parameters

Transmission line models

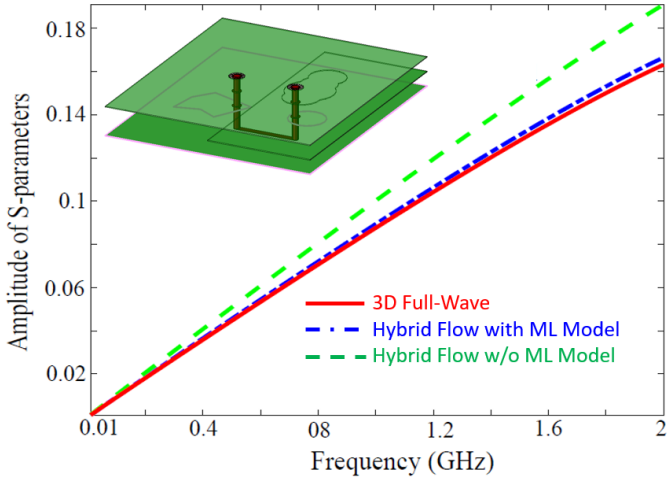
ML Model for Via Structure

The multi-layer perceptron (MLP) regressor model is trained and applied to calculate equivalent circuit elements of via structures.



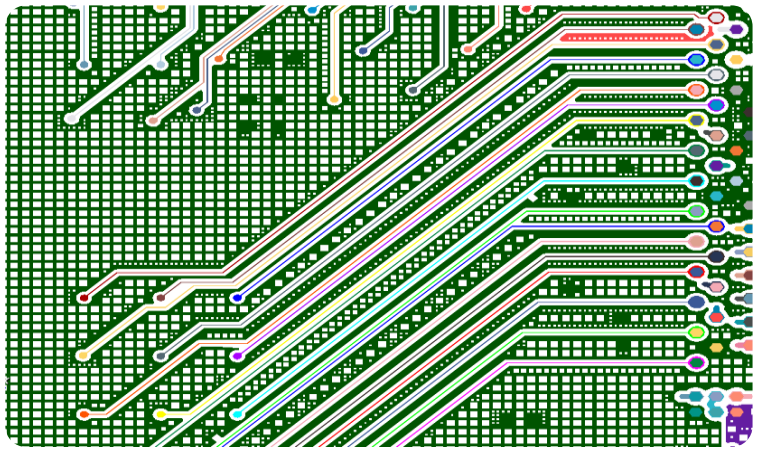


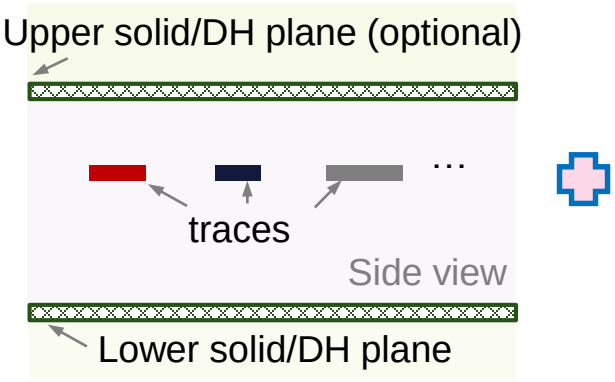
Trace-via-trace transition region



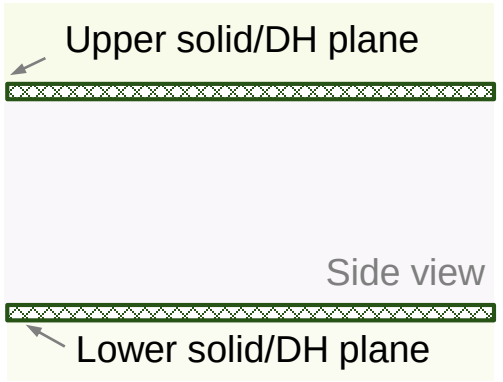
ML Model for Planes with Degassing Hole

- Difficulties in modeling degassing hole (DH)
  - ➢ Thousands to millions of degassing holes per metal layers
  - ➢ Essentially a 3D problem needs full-wave simulation
  - ➢ Needs to consider parallel-planes field domain and trace over and between degassing hole planes to characterize both signal integrity (SI) and power integrity (PI)





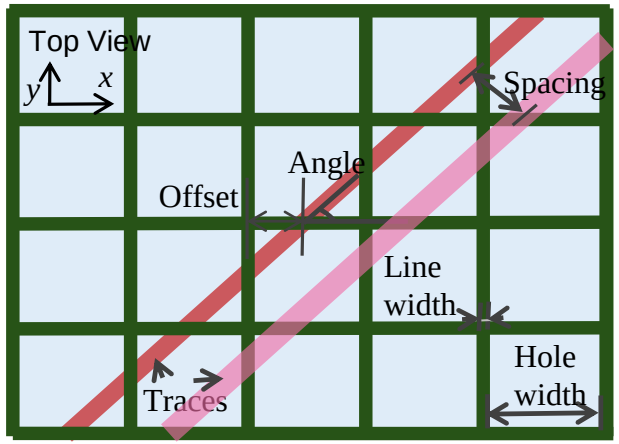
Trace-over/between-DH plane for SI

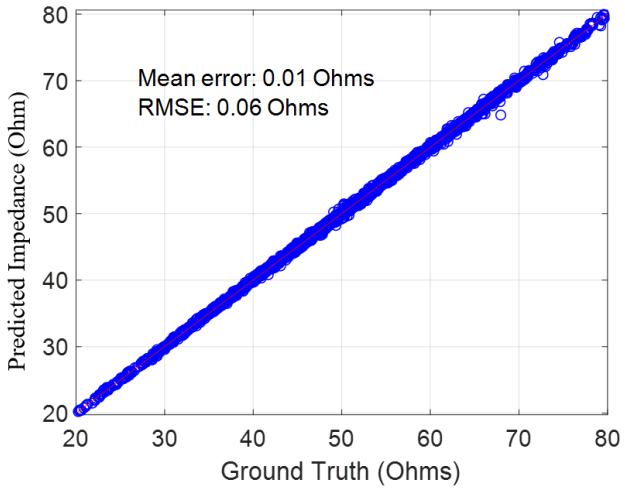


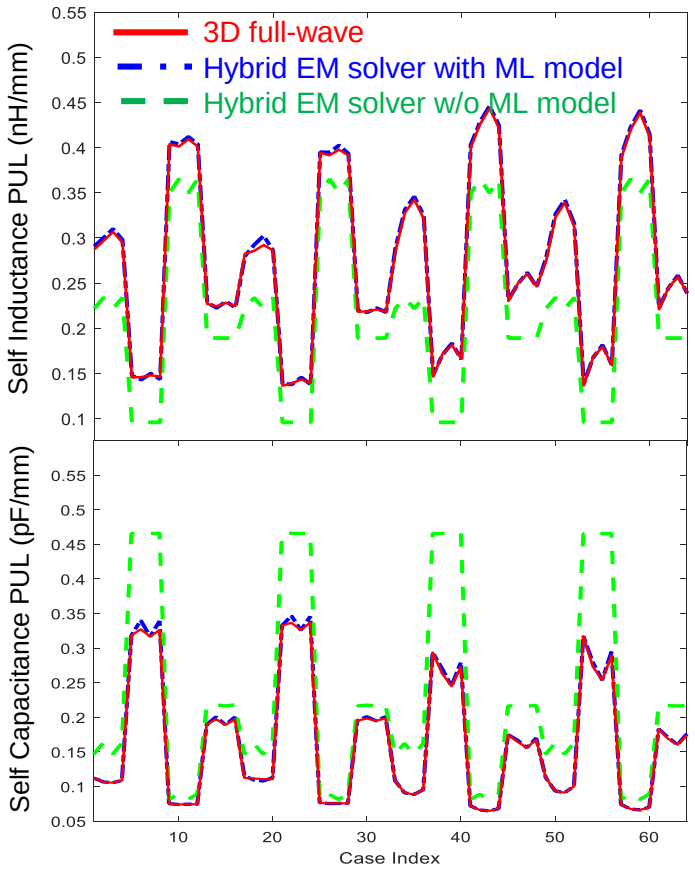
Parallel planes with DH for PI

ML Model for Traces with DH Planes

- Artificial neural network (ANN) model trained by 3D full-wave data is applied for trace with DH reference plane modeling
  - ➢ Hybrid solver with ML model: no need to mesh DH lines
  - ➢ Unparallelly efficiency with good accuracy

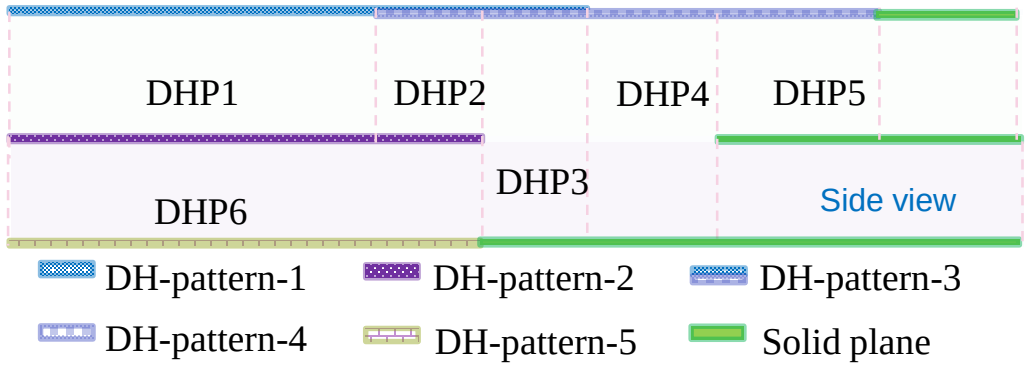




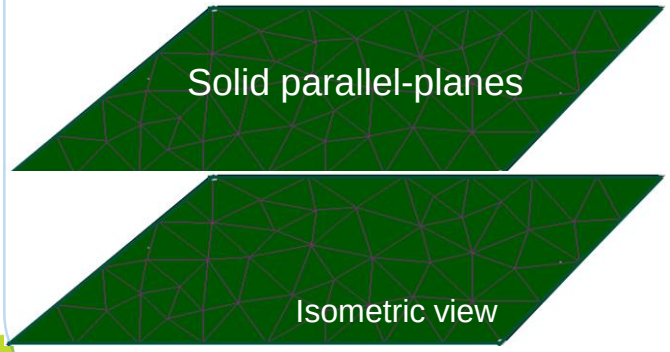


ML Model for Parallel Planes with DH

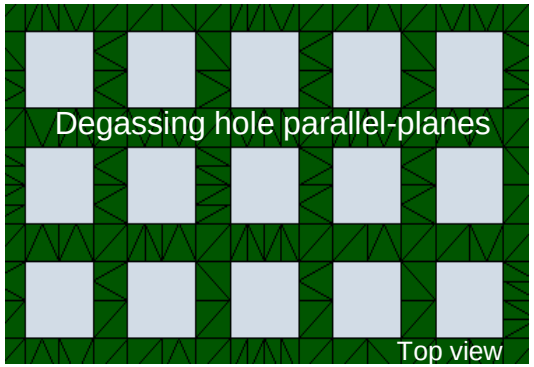
- Parallel-planes with DH field domain modeling
  - ➢ Degassing hole parallel planes (DHPs) will be detected according to boundaries of degassing hole regions in adjacent metal layers
  - ➢ Hybrid EM solver with 3D full-wave data trained ANN model is applied

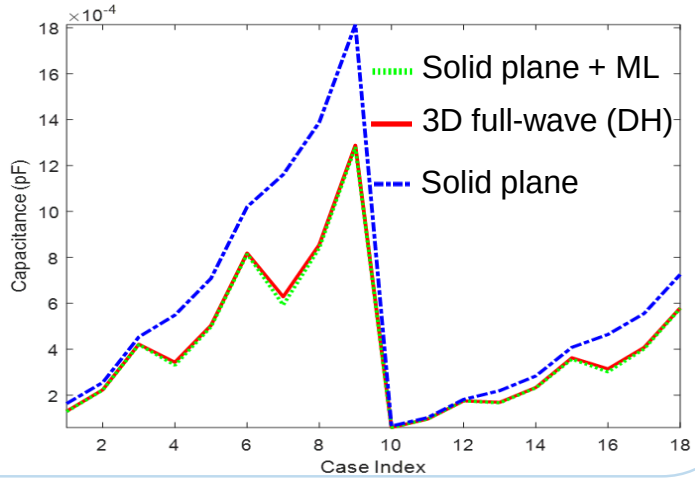


FEM in hybrid EM solver
(no mesh for DH lines)



ML model trained by 3D full-wave data

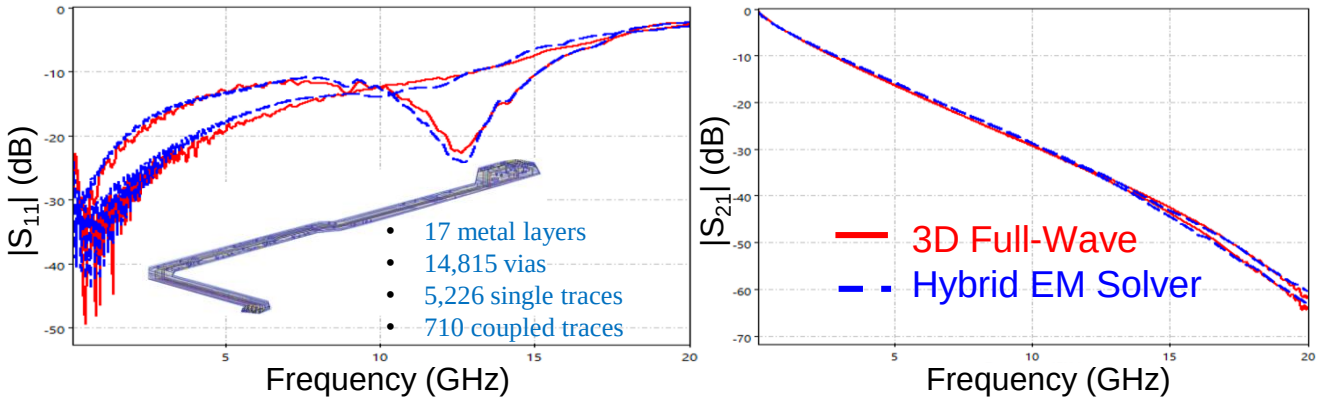




Performance and Validation

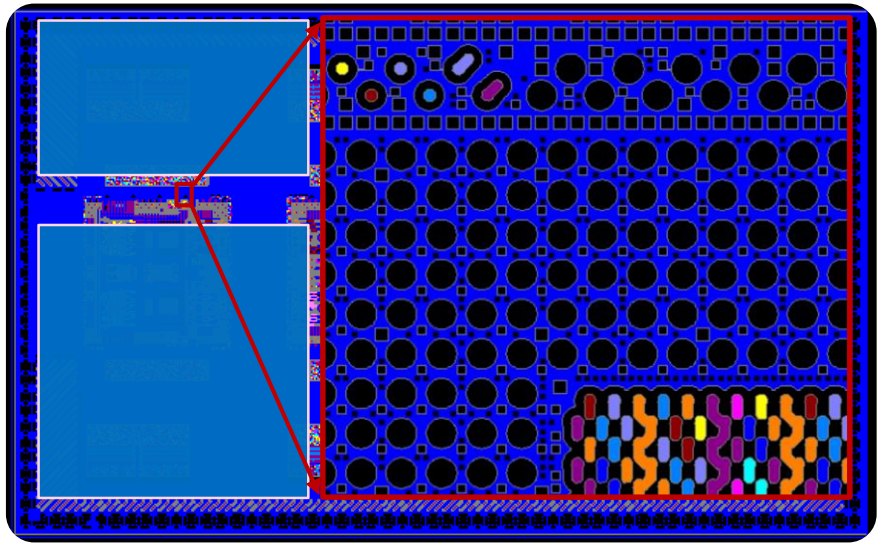
The hybrid EM solver, leveraging the AI/ML techniques, has the capability to do the extraction of entire IC package with high efficiency and reliability.

Part of a layered interconnector



EM Solver	CPU Number	Simulation Time	Memory
3D full-wave	72	47 hrs. 11 mins.	374 GB
Hybrid EM solver	40	53 mins.	148 GB

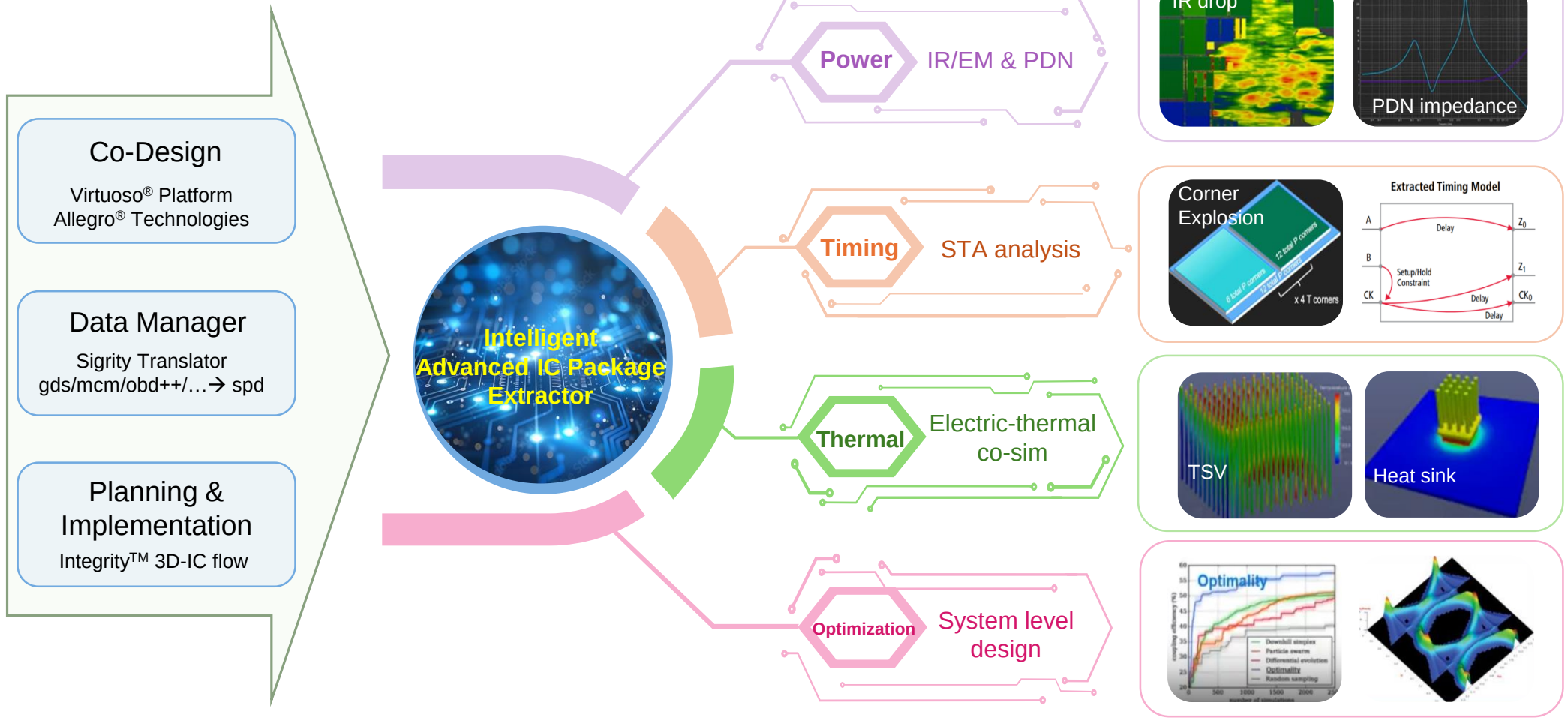
CoWoS-L design



Components	17 (Die + LSI + BGA)
Number of Vias	~4.3M
Degassing holes	~2.4M
Run time	~15 hrs.

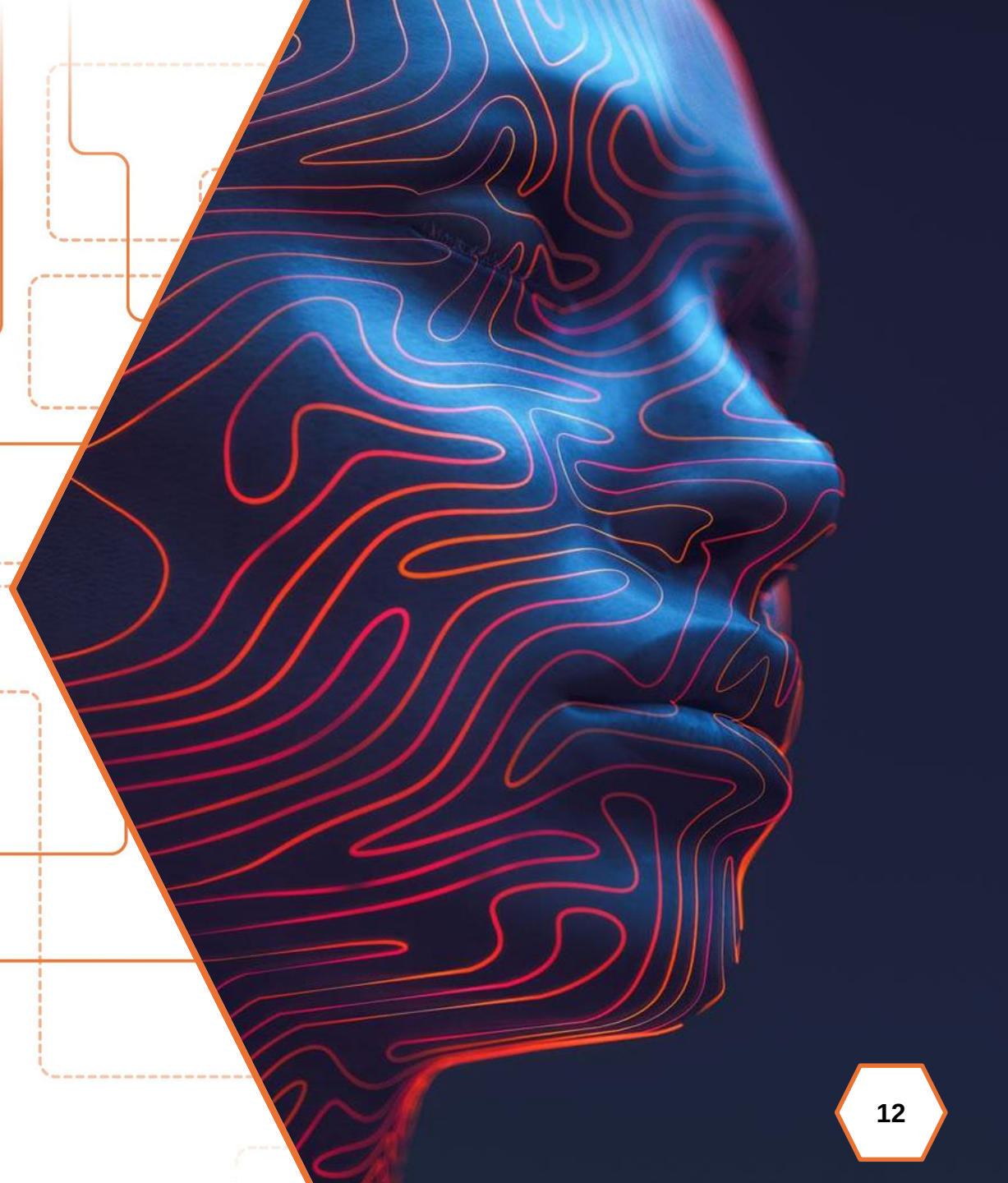
System and Co-Design Automation Flow

- Model interface auto-connecting and die to package auto-mapping



Summary

- High performance hybrid electromagnetic solver to fully utilize the advantages of basic EM methods (~10x to >100x speedup)
- 3D full-wave data trained ML models for fast and accurate modeling
- System-level co-design automation flow for convenient extraction and analysis
- Overnight comprehensive extraction of entire design to meet compressed schedules



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